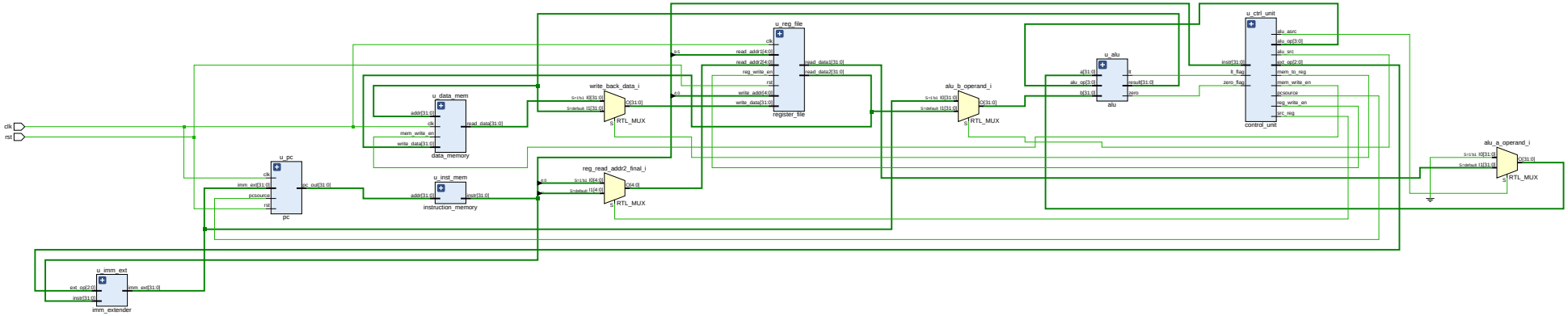
clk
rst
u_pc
clk
imm_ext[31:0]
pcsource
rst
pc_out[31:0]
pc
u_imm_ext
ext_op[2:0]
instr[31:0]
imm_ext[31:0]
imm_extender
u_data_mem
addr[31:0]
clk
mem_write_en
write_data[31:0]
read_data[31:0]
data_memory
u_inst_mem
addr[31:0]
instr[31:0]
instruction_memory
write_back_data_i
S=1'b1 I0[31:0]
S=default I1[31:0]
O[31:0]
S
RTL_MUX
reg_read_addr2_final_i
S=1'b1 I0[4:0]
S=default I1[4:0]
O[4:0]
S
RTL_MUX
u_reg_file
clk
read_addr1[4:0]
read_addr2[4:0]
reg_write_en
rst
write_addr[4:0]
write_data[31:0]
read_data1[31:0]
read_data2[31:0]
register_file
alu_b_operand_i
S=1'b1 I0[31:0]
S=default I1[31:0]
O[31:0]
S
RTL_MUX
u_alu
a[31:0]
alu_op[3:0]
b[31:0]
lt
result[31:0]
zero
alu
u_ctrl_unit
instr[31:0]
lt_flag
zero_flag
alu_asrc
alu_op[3:0]
alu_src
ext_op[2:0]
mem_to_reg
mem_write_en
pcsource
reg_write_en
src_reg
control_unit
alu_a_operand_i
S=1'b1 I0[31:0]
S=default I1[31:0]
O[31:0]
S
RTL_MUX